REMARKS

Applicants thank the Examiner for examining the claims of the present application. As more fully explained below, applicants are adding claims 48-60. With entry of these amendments, claims 1-60 will remain pending in the application. Applicants respectfully request reconsideration of the Examiner's rejections in view of the following amendments and remarks.

Rejection of claims 1-47 under 35 U.S.C. § 102(b)

The second Office action rejects claims 1-47 under 35 U.S.C. § 102(b) as being anticipated by Rajski et al., "Test Data Decompression for Multiple Scan Designs with Boundary Scan," 47 IEEE Transactions on Computers (November 1998) (the "Rajski article"). Specifically, the Examiner contends that the Rajski article recites the claim limitations of "providing a compressed test pattern of bits; decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided; and applying the decompressed test to scan chains of the circuit under test." This rejection is respectfully traversed.

Claim 1

Claim 1 requires "decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided." The decompressors disclosed by the Rajski article do not decompress the compressed test pattern "as the compressed test pattern is being provided." Instead, as was confirmed by Dr. Rajski (the principal author of the Rajski article), the cited Rajski article discloses loading the compressed test pattern into the decompression hardware and decompressing the compressed test pattern occur at separate, independent stages of operation.

Section 2.4 and FIG. 5 of the Rajski article describe the operation of the model decompressor disclosed therein. As seen in FIG. 5, the model decompressor includes a "*Load seed*" signal and a "*Decompression*" signal, which are used to control the operational mode of the decompressor. The decompressor operates in one of three modes: (1) a pseudorandom mode (in which the load seed and decompression signal are both 0); (2) a shift mode (in which the load seed signal is 1 and the decompression signal is 0); and (3) a decompression mode (in which the

decompression signal is 1 and the load seed signal is 0). *See* Rajski article at p. 1192, col. 2, ll. 47-58. The Rajski article explains the actual operation of the model decompressor as follows:

1) Reset the MP-LFSR including the flip-flops shared with the scan.
2) Switch to the shift mode.
3) Shift the seed with the polynomial ID being appended
4) Switch to the decompression mode.
5) Decompress the test vector by applying L clock cycles to the MP-LFSR.
6) Switch to the functional mode.
7) Apply the test vector to the circuit under test.
8) Shift out the response to the test response analyzer.

Rajski article, p. 1193, col. 1, ll. 3-12 (emphasis added).

Thus, the model decompressor first receives the compressed test pattern in a shift mode, then decompresses the compressed test pattern in a decompression mode that occurs after and separate from the shift mode.

The two-dimensional decompression hardware disclosed in the Rajski article also decompresses a test pattern in two separate, independent stages. As shown in FIG. 6, the two-dimensional decompression hardware also includes a "*Load seed*" signal and a "*Decompression*" signal for controlling the various stages of decompression. The Rajski article explains: "By controlling the *Load seed* and *Decompression* signals, the variable-length seeds are loaded one by one and decompressed. The seeds are loaded by shifting the seed variables serially. Once the seed is loaded, decompression is performed in parallel through the XOR network." Rajski article at p. 1196, col. 1, ll. 26-31 (emphasis added). Moreover, as shown in FIG. 8 of the Rajski article, test patterns are loaded and decompressed in this same manner in the boundary-scan environment. *See also* Rajski article at p. 1198, col. 2, ll. 20-38; p. 1199, col. 1, ll. 1-9.

Accordingly, the decompressors disclosed in the Rajski article do not decompress the test pattern "as the compressed test pattern is being provided," as required by claim 1 of the present application. Claim 1 is therefore in condition for allowance, and the 35 U.S.C. § 102(b) rejection should be removed.

Claims 2-18, 39-41

Claims 2 through 18 and claims 39 through 41 depend from claim 1 and should be in condition for allowance for at least the reasons stated above. Claims 2 through 18 also set forth independently patentable inventions.

Claims 19-29, 34-38, 42, and 43

Claims 19-21 disclose a "means for decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided." Claims 22-29, 42, and 43 disclose a "decompressor adapted to receive a compressed test pattern of bits and decompress the test pattern into a decompressed test pattern of bits as the compressed test pattern is being received." Claims 34-35 disclose a "decompressor coupled to the storage, the decompressor adapted to receive a compressed test pattern of bits provided from the storage and to decompress the test pattern into a decompressed test pattern of bits as the compressed test pattern is being received." Claims 36-38 disclose "decompressing within the test the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided." Accordingly, claims 19-29, 34-38, 42, and 43 should be in condition for allowance for at least the reasons stated above with respect to claim 1. Claims 19-29, 34-38, 42, and 43 also set forth independently patentable inventions.

Claim 30

Independent claim 30 requires that the decompressor have a "plurality of input channels" that receive "in parallel" the bits of the compressed test pattern. By contrast, the decompressors disclosed in the Rajski article receive bits of the compressed test pattern serially, not in parallel.

As seen in FIG. 5 of the Rajski article, the multiplexer controlled by the *Load seed* signal serially loads the model decompressor with the compressed test pattern ("Poly ID") when the *Load seed* signal is activated. The Rajski article explains: "To handle the seeds, a multiplexer placed at the input side of the MP-LFSR allows the seeds to be serially shifted." Rajski Article, p. 1192, ll. 37-39 (emphasis added). Likewise, in the two-dimensional decompressor shown in FIG. 6 of the Rajski article, the multiplexer coupled to the Test Data Input ("TDI") serially loads the compressed test pattern into the decompressor when the *Load seed* signal is activated. Further, the network of XOR and AND gates in FIG. 6 control the feedback between the scan chains so that "a serial path through the decompressor is created." *Id.* at p. 1196, ll. 7-10 (emphasis added). The Rajski article explains: "By controlling the *Load seed* and *Decompression* signals, the variable-length seeds are loaded one by one and decompressed. The seeds are loaded by shifting the seed variables serially." *Id.* at p. 1196, ll. 27-30 (emphasis

added). Moreover, as shown in FIG. 8 of the Rajski article, the test patterns are also loaded serially in the boundary-scan environment.

Accordingly, the decompression hardware disclosed by the Rajski article does not have a "plurality of input channels" that receive "in parallel" the bits of the compressed test pattern as required by claim 30. Claim 30 is therefore in condition for allowance, and the 35 U.S.C. § 102(b) rejection should be removed.

Claims 31, 44, and 45

Dependent claims 31, 44, and 45 depend from claim 30 and should be in condition for allowance for the reasons stated above. Claims 31, 44, and 45 also set forth independently patentable inventions.

Claim 32

Claim 32 requires that the linear finite state machine be adapted to "logically combine bits stored within the machine with bits received from a compressed test pattern." By contrast, the decompressor of the Rajski article has separate, independent stages for shifting and decompressing the compressed test pattern, and is completely disconnected from incoming test patterns during the decompression stage.

As explained above, the decompressor disclosed by the Rajski article operates in one of three modes: (1) a pseudorandom mode; (2) a shift mode; and (3) a decompression mode. *See* Rajski article at p. 1192, col. 2, ll. 47-58. Before shifting a compressed test pattern into the decompressor, "the content of the whole LFSR [is cleared] before the seeds are loaded." Rajski article, p. 1192, col. 2, ll. 39-42. During the shift mode, the compressed test pattern is serially shifted into the decompressor via a multiplexer (in FIG. 5, the multiplexer with the "Poly ID" input port, and in FIG. 6, the multiplexer with the "TDI" input port). *Id.* at p. 1192, col. 2, ll. 50-54. During the decompression mode, the multiplexer is disconnected from the Poly ID or TDI input port and switched to receive a feedback signal from within the decompressor. *Id.* at p. 1192, col. 2, ll. 33-37. Thus, during the shift mode, the compressed pattern is loaded into the decompressor without modification, and during the decompression mode, the decompressor cannot receive any bits of a compressed pattern.

Accordingly, the decompression hardware disclosed by the Rajski article is not adapted to "logically combine bits stored within the machine with bits received from a compressed test pattern" as required by claim 30. Claim 30 is therefore in condition for allowance, and the 35 U.S.C. § 102(b) rejection should be removed.

Claims 33, 46, and 47

Claims 33, 46, and 47 depend from claim 32 and should be in condition for allowance for at least the reasons stated above. Claims 33, 46, and 47 also set forth independently patentable inventions.

New Claims 48-60

Applicants are adding new claims 48-60.

CONCLUSION

For the reasons stated above, it is believed that the application is in condition for allowance, and such action is respectfully requested. If any further issues remain concerning this application, the Examiner is invited to call the undersigned to discuss such matters.

Respectfully submitted,

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